



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Yutoshi AOKI**

Attorney Docket 40301/0578

Title: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING  
INSULATED GATE FIELD EFFECT TRANSISTOR AND METHOD  
OF MANUFACTURING THE SAME

Appl. No.: 09/440,928

Filing Date: November 16, 1999

Examiner: S. Rao

Art Unit: 2814

RECEIVED  
OCT -4 2002  
TECHNOLOGY CENTER 2800

#19/Evt.  
Marsha  
10/10/02

**PETITION FOR EXTENSION OF TIME**  
**UNDER 37 C.F.R. § 1.136**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

It is respectfully requested that an extension of time for the period indicated below be granted in accordance with the provisions of 37 C.F.R. § 1.136 to take the action required in the application identified in caption, as reflected by the papers submitted herewith.

<u>X</u>	First Month	\$ 110	(\$ 55)*
10/02/2002 CNGUYEN 0000033 09440928 —	Second Month	\$ 290	(\$145)*
01 FC:115	Third Month	\$ 520	(\$260)*
<b>TOTAL FEE: \$110.00</b>		*(Small Entity)	

A check in the amount of the above Total Fee is attached. This amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741. If one or more (additional) extension(s) of time is/are required for the filing of this paper, such extension(s) is/are hereby expressly petitioned for and the Commissioner is authorized to charge the required fee to Deposit Account No. 19-0741.

Respectfully submitted,

September 30, 2002  
Date

Aaron C. Chatterjee  
Aaron C. Chatterjee  
Reg. No. 41,398

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